Test Method of Memory IC Function on Device Board with Dynamic Competing Cycle

Background of the Invention

The present invention relates to a method of estimating a function of a memory IC on a board of a device (hereinafter, referred to as a lower device), connected to a controller by a communication interface not especially specified, capable of receiving a control therefrom.

Hitherto, in order to estimate the IC function on a board of a lower device, a controller is connected to a communication interface of the lower device, simulated control software is activated on the controller, built-in software for the estimation of the memory IC function is downloaded from the controller to the lower device, and the controller gives an instruction to the built-in software for the estimation of the memory IC function on the lower device, thereby performing a separate function test and a competing function test combined with a plurality memory ICs on a plurality of memory ICs (Flash ROM, SRAM, SDRAM) installed on the board of the lower device.

In the competing function test of the memory ICs (Flash ROM, SRAM, SDRAM) installed on the board of the lower device, according to the built-in software for the estimation of the

memory IC function on the lower device, however, the competing timing is fixed, namely, when a test of a memory IC of a predetermined size is finished, it is switched to a test of another memory IC, and accordingly, there is such a problem that a test of the actual competing timing occurring in real circumstances can not be realized. Therefore, there have been cases that failures after the shipment of the boards built in products.

Summary of the Invention

The invention is to solve the above problem by dynamically varying the competing timing to any cycle in the competition test of a plurality of memory ICs (Flash ROM, SRAM, SDRAM) installed on a board of the lower device by the built-in software for the estimation of the memory IC function on the lower device.

In a test method of a memory IC function according to this invention, memory ICs of different types are prepared after a memory tester is prepared. The data related to each test method of these memory ICs is transmitted to the memory tester. Further, after a random number is generated, a test of a predetermined memory IC is executed in reply to the generated random number. When it is checked whether the tests of all the memory ICs are finished or not, the generation of

the random number and the execution of the test are repeated, when they are not finished, while when they are finished, the processing is finished.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram for describing the structure of a test method of this invention.

Fig. 2 is a block diagram showing the structure of a function test of a memory IC.

Fig. 3 is a first flow chart for describing the operation procedure of the test method of this invention.

Fig. 4 is a second flow chart for describing the operation procedure of the test method of this invention.

Fig. 5 is a third flow chart for describing the operation procedure of the test method of this invention.

Fig. 6 is a fourth flow chart for describing the operation procedure of the test method of this invention.

Fig. 7 is a fifth flow chart for describing the operation procedure of the test method of this invention.

Fig. 8 is a sixth flow chart for describing the operation procedure of the test method of this invention.

Fig. 9 is a view showing an input screen of command transmission data.

Fig. 10 is a view showing a screen displaying the estimation result of a memory IC.

Fig. 11 is a view for describing the operation concept of the test method of this invention.

Fig. 12 is a view for describing the operation concept of the test method of this invention in detail.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the form of an embodiment in a test method of the invention will be described according to the drawings.

Fig. 1 is a block diagram for describing the structure of a test method in this embodiment. A controller 1 is connected to a lower device 3 by a communication interface 2 not especially specified. An input device 4, for example, a keyboard and a mouse, not especially specified, and a display 5, for example, a CRT, not specified, are connected to the controller 1, thereby enabling the input/output operation to/from the controller 1.

The controller 1 includes an operating system 12 not especially specified and a lower device controlling system 11 that is the software running on this operating system. The lower device controlling system 11 comprises command transmission data input processing 11a for inputting the command transmission data for controlling the lower device 3 from the communication interface 2, command execution result display processing 11b for displaying the execution

result in the lower device 3 toward the command transmission data, to a user, and communication processing 11c for realizing a communication protocol not especially specified.

The lower device 3 includes a real time operating system 32 for a built-in system not especially specified and a memory IC function estimation system 31 that is the built-in software running on this real time operating system. The memory IC function estimation system 31 comprises command analyzing processing 31a for analyzing the command transmission data from the controller 1 and activating the function test processing of a memory IC, memory IC function test processing 31b for executing the function test of a memory IC, memory IC function test execution controlling processing 31c for controlling the execution order of the memory IC function tests, timer interruption processing 31d periodically activated at arbitrary time, random number generation processing 31e for generating any random number, not especially described, transmission data edit processing 31f for editing the execution result of the memory IC function test in a format displayable in the controller 1, and communication processing 31g for realizing a communication protocol not especially specified.

The operation procedure of the test processing of the memory IC function estimation system, in this embodiment, will be hereinafter described in detail by referring to the

drawings. Fig. 2 is a block diagram showing the structure of the memory IC function test processing; Fig. 3 is a schematic flow chart of the operation procedure of the controller 1; Fig. 4 is a schematic flow chart of the operation procedure of the lower device 3; Fig. 5 is a schematic flow chart of the estimation test of a plurality of memory ICs; Fig. 6, Fig. 7, and Fig. 8 are schematic flow charts of the timer interruption processing; Fig. 9 is a command transmission data input screen; and Fig. 10 is a display screen of the memory IC estimation result.

At first, the operation procedure for estimating a memory IC in the controller 1 will be described. Fig. 9 is a view showing a screen of entering a command for controlling the lower device 3 or a test No for the estimation of a memory IC. On this screen, a user enters a command for controlling the lower device 3 or a test No for the estimation of a memory IC by using the input device 4 not specified (STEP 1). Thereafter, the user presses "Enter Key" by using the input device 4, thereby transmitting the transmission data corresponding to a command for controlling the lower device 3 or a test No for the estimation of a memory IC, from the controller 1 to the lower device 3 through the communication interface 2 (STEP 2). Next, the data from the lower device 3 is received through the communication interface 2 and the display screen of the memory IC estimation execution result

shown in Fig. 10 is shown on the display 5 as the memory IC estimation execution result (STEP 3).

Now, the operation procedure in executing the estimation operation of a plurality of memory ICs in the lower device 3 will be described. When the lower device 3 receives the transmission data corresponding to the test No for the estimation of the memory IC, from the controller 1 through the communication interface 2, the transmission data from the controller 1 is analyzed in the command analyzing processing 31a (STEP 4).

When the analyzed result is the estimation test No of a single memory IC, the corresponding memory IC function test processing 31b is executed (STEP 5). After completion of the test, the transmission data of the test execution result to the controller 1 is created in the transmission data edit processing 31f and the test execution result is transmitted to the controller 1 through the communication processing 31g and the communication interface 2 (STEP 6).

When the analyzed result is the estimation test No of several n (0<n<) memory ICs, at first, the numeric value t1 (0<t1<255) is taken out in the random number generation processing 31e for generating arbitrary random number (STEP 7). Next, the timer interruption processing 31d with the taken out numeric value t1 being defined as a cycle (millisecond) is activated (STEP 8). At the same time, the estimation test of the first

memory IC is activated in the memory IC function test processing 31b1 (STEP 9). In the timer interruption processing 31d to be generated after t1 millisecond, the memory IC function test processing 31b1 executing the estimation test of the first memory IC is interrupted by the memory IC function test execution controlling processing 31c for controlling the execution order of the memory IC function tests, and the estimation test of the second memory IC is activated according to the memory IC function test processing 31b2 (STEP 10). Thereafter, the numeric number t2 (0<t2<255) is taken out by the random number generation processing 31e for generating arbitrary random number and the timer interruption processing 31d with t2 being, defined as a cycle (millisecond) is activated (STEP 11).

Similarly, in the timer interruption processing 31d with t(n-1) being defined as a cycle (millisecond), which is taken by the random number generation processing 31e for generating arbitrary random number, the memory IC function test processing 31b(n-1) executing the estimation test of the (n-1)-th memory IC is interrupted by the memory IC function test execution controlling processing 31c for controlling the execution order of the memory IC function tests, and the n-th memory IC estimation test is activated according to the memory IC function test processing 31bn (STEP 12). Thereafter, the numeric value tn (0<tn+1<255) is taken out according to the

random number generation processing 31e for generating arbitrary random number and the timer interruption processing 31d with tn being defined as a cycle (millisecond) is activated (STEP 13).

When activating the n-th memory IC estimation test, in the timer interruption processing 31d to be generated after tn millisecond, the memory IC function test processing 31bn executing the estimation test of the n-th memory IC is interrupted according to the memory IC function test execution controlling processing 31c for controlling the execution order of the memory IC function tests, and the estimation test of the first memory IC is resumed after releasing the interrupted state according to the memory IC function test processing 31b1 (STEP 14). Thereafter, the numeric value t (n+1) ($0<tn+1<255$) is taken out by the random number generation processing 31e for generating arbitrary random number and the timer interruption processing 31d with t(n+1) being defined as a cycle (millisecond) is activated (STEP 15).

Thus, after the estimation tests of the first to the n-th memory ICs have been activated, taking out the random number, activating the timer interruption processing, and interruption of the estimation test of each memory IC during the timer interruption processing and resumption of the estimation test are repeatedly until the estimation tests of

all the memory ICs are finished.

After finishing the estimation tests of all the memory ICs, the transmission data of the test execution result to the controller 1 is created in the transmission data edit processing 31f, and the test execution result is transmitted to the controller 1 through the communication processing 31g and the communication interface 2 (STEP 6).

As mentioned above, according to the embodiment, in the competing function test of a plurality of memory ICs (Flash ROM, SRAM, SDRAM) installed on a board of the lower device, the competing timing can be dynamically changed, and the competing function test of the memory ICs (Flash ROM, SRAM, SDRAM) can be achieved under the condition extremely close to the competing timing generated in real circumstances.

Now, a second embodiment will be described. The second embodiment is constituted by adding IC (for example, UART, USB, DMAC) installed on the device board other than the memory IC, as the competing IC in the first embodiment.

Namely, it performs the operation with the other IC (for example, UART, USB, DMAC) installed on the device board added to the subject of IC competing in the memory IC function estimation system of the first embodiment.

Fig. 11 is a view for describing the operation concept of a test method according to the second embodiment.

Fig. 12 is a view for describing the operation concept of the test method in detail according to the second embodiment.

A STOP issuing function of the second embodiment has the following restrictions.

The STOP is not issued during the DMA transfer, SIO transfer, and UART transfer.

After completion of the restriction processing, PPWC task (STOP) is immediately activated.

Accordingly, the following processings are performed in the second embodiment.

The PPWC task (STOP) is activated not according to the management of the scheduler but according to the task to be restricted.

A post call to the PPWC task (STOP) is issued only from the DMAC/SIO/UART task.

The STOP operation will be described referring to Fig. 12 as follows.

① Register setting and mask release of DMAC is performed

and the DMA transfer (cycle steal) is executed.

② The processing time of the scheduler is extended during the DMA transfer (cycle steal).

③ The PPWC task is in a waiting state (wait) for post from the DMAC/SIO/UART task.

④ The interruption of the transfer completion is issued from the DMAC.

⑤ The DMAC task issues the post to the PPWC task.

⑥ The PPWC task executes the STOP processing.

⑦ The STOP state. Though the timer is operating, interruption is not supplied because the HCLK is stopped.

⑧ The ** interruption is supplied. The hardware transits from the STOP state into the RUN state.

This interruption is received and abandoned by an interruption handler.

⑨ Since it comes into the RUN state, the HCLK begins to move and an interruption is supplied from the timer.

Upon receipt of the timer interruption, the scheduler processing is performed.

As mentioned above, according to the embodiment, in the competing function test of a plurality of memory ICs (Flash ROM, SRAM, SDRAM), communication interface IC (UART, USB), and CPU peripheral IC (DMAC) installed on a board of the lower device, the competing timing can be dynamically changed, and

the competing function test of the memory ICs (Flash ROM, SRAM, SDRAM), communication interface IC (UART, USB), and CPU peripheral IC (DMAC) can be achieved under the condition extremely close to the competing timing generated in real circumstances.